#### REMARKS

In response to the above-identified Office Action, no claims are amended, Claim 10 is cancelled and no claims are added. Accordingly, Claims 1-9 and 11-24 are pending. Claims 1-24 are rejected. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

## I. <u>Drawings</u>

The Examiner has rejected the drawings for failing to comply with 37 CFR §1.84(p)(5) because reference numerals included in the specification were omitted from the figures. Regarding reference elements 128 and 130, Applicants submitted a Preliminary Amendment to the Patent Office on December 7, 2000 (received by OIPE on December 11, 2000) wherein a replacement FIG. 3 was attached. Replacement FIG. 3 contained elements 128 and 130. At the request of the Examiner, Applicants resubmitted their Preliminary Amendment on July 6, 2004.

### II. In the Specification

The Examiner has objected to the specification for containing two minor informalities. Applicants have made the requisite corrections to the specification, and therefore request that the Examiner withdraw the objection to the specification.

## III. <u>Double Patenting Rejection</u>

Claims 1-9 and 12-21 are provisionally rejected by the Examiner under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-19 of copending Application No. 09/705,678. Applicants hold in abeyance this rejection until such time as the claims on which the rejection is premised are granted.

# IV. Claim Rejections Under 35 U.S.C. §112

The Examiner rejects Claim 10 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In response, Claim 10 is cancelled.

## V. Claim Rejections Under 35 U.S.C. §103

The Examiner rejects Claims 1-4, 6-12, 19-20 and 22-24 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,966,544 issued to Sager ("Sager") in view of U.S. Patent No. 3,603,934 issued to Heath ("Heath"). Applicants respectfully traverse this rejection.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or

042390.P9576 -7- 09/705,668

suggest all the claim limitations. (MPEP §2142) For the reasons provided below, the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record.

Regarding Claim 1, Claim 1 includes the following claim feature, which is neither taught nor suggested by either <u>Sager</u>, <u>Heath</u> or the references of record:

a scheduler coupled between the replay queue and the execution unit to speculatively schedule instructions for execution, to <u>in</u>crement a counter for each of the plurality of instructions to reflect the number of times each of the plurality of instructions has been executed, and to <u>dispatch</u> each <u>instruction</u> of the plurality of instructions to the execution unit either <u>when</u> the <u>counter does not exceed</u> a <u>maximum number of replays</u> or, <u>if</u> the <u>counter</u> for the instruction <u>exceeds</u> the <u>maximum</u> number of <u>replays</u>, <u>when the instruction is safe to execute</u>. (Emphasis added.)

Conversely, <u>Sager</u> describes a technique to <u>prevent thread deadlock</u> by assigning threads alternating priority using an alternating priority scheme. Namely:

Therefore, it is necessary to have a flexible and dynamic alternating priority scheme in which each thread is alternately given priority for some sufficient period of time in order for it to make progress, which in turn can help the other thread make progress. More specifically, each thread is to be alternately given the priority for some period of time initially. . . . As each thread is being executed, its progress is monitored to determine whether it is being stuck. If a particular thread, for example thread 0, has not made any progress in the period of time during which it has priority, then it will be given priority for a longer duration of time the next time it has priority. (See col. 9, lines 3-18.) (Emphasis added.)

As indicated by the Examiner, <u>Sager</u> has not taught the above-recited features of Claim 1. Accordingly, the Examiner has cited <u>Heath</u>. According to the Examiner:

Heath has taught the general idea of when an instruction is erroneously executed, the instruction will be re-executed a predetermined number of times and when that number is executed, corrective measures have to be taken. (Heath, col. 2, lines 1-14.) A person of ordinary skill in the art would recognize that by using the idea of <u>Heath</u>, a counter could be implemented in <u>Sager</u> so that a predetermined number of replays are attempted, thereby trying to solve the execution error through re-execution. However, when the predetermined number is exceeded, the re-execution of the erroneous instruction would be suspended so that other instructions, which would possibly execute correctly, would use the system resources instead of the continuously erroneous instruction. . . . Therefore, it would be obvious to one of ordinary skill in the art at the time the invention was made to incorporate the counter and error correction of <u>Heath</u> in the device of <u>Sager</u> to execute other instructions instead of the erroneous instructions, thereby increasing processor efficiency. (pg. 11, ¶1 - pg. 12, ¶1 of Office Action mailed July 9, 2004.)

Applicants respectfully disagree with the Examiner's contention. In fact, Applicants respectfully submit that preventing thread deadlock by assigning threads alternating priority using an alternating priority scheme as taught by <u>Sager</u>, as well as the above-recited features of Claim 1, lack any similarity to sustain an argument that there is a suggestion or motivation to modify the reference or combine the reference teachings of <u>Sager</u> in view of <u>Heath</u>.

### As described within **Heath**:

During the execution of any of these steps, it is possible that there may be a malfunction in the system. Malfunctions, or errors, can be either short-lived (transient) or long-lived (solid). A transient error may for example be the result of a sudden fluctuation in the power supply or the result of a mechanical shock. Failure of a component, such as a transistor or diode may result in a solid error. (col. 1, lines 27-34.)

As further described within the passage cited by the Examiner:

In most systems wherein an attempt is made to re-execute an instruction during the course of which an error has been detected, after a predetermined number of unsuccessful attempts to re-execute the instruction, the error would be classified as solid and the system would signal the operator that corrective action was necessary. (col. 2, lines 3-13.) (Emphasis added.)

# Accordingly, <u>Heath</u> describes a system wherein:

Detection of a <u>malfunction of a functional unit</u> (e.g., a parity error) will cause the system to determine whether one-half of the unit is functioning properly. If one-half of the unit is functioning properly, then the good half of the unit will be used twice processing one-half of the data word each time to produce a correct result. . . . The recursive splitting of the functional unit may be continued to any desired limit, but it will generally be preferable not to use a smaller portion of the functional unit than the smallest portion thereof which can be checked for errors. (col. 2, lines 51-71.)

Based on the cited passages above, Applicants respectfully submit that the teachings of <u>Heath</u> are strictly limited to actions taken in response to a detected hardware malfunction. As indicated, if the malfunction is solid, corrective action by an operator is required. Accordingly, Applicants respectfully submit that the teachings of <u>Heath</u> are directed to actions to be taken in response to hardware malfunctions.

Conversely, the features of Claim 1 are directed to speculatively executed instructions.

Unsuccessful execution of speculative such instructions does not occur due to hardware malfunctions, but instead would occur, for example, when the speculative execution uses invalid data. In such situations, the instruction may be re-executed such that during subsequent execution, the instruction processes valid data. In other words:

Data speculation may involve speculating that data from the execution of instruction in which the present instruction is dependent will be stored in the location in cache memory such that the data in the cache memory will be valid by the time the instruction attempts to access the location in cache memory. The dependent instruction is dependent on the result of a load of the result of the instruction on which it is dependent. When the load misses the cache, the dependent instruction must be re-executed. (See, col. 2, lines 6-11 of Applicants' specification.)

As indicated above, the teachings of <u>Sager</u> are directed to situations where a processing priority between threads is used to indicate which one of the two threads is to have priority if both

threads compete for a particular resource in order to make progress. (*See*, col. 10, lines 39-42.) In other words, the above-recited features of Claim 1, as well as the teachings of <u>Sager</u>, do not involve situations regarding failed execution of instructions due to hardware malfunctions, nor the recursive splitting of functional units to identify a properly functioning portion.

Accordingly, Applicants respectfully submit that one skilled in the art would not combine the teachings of <u>Sager</u> in view of <u>Heath</u> since there is a complete lack of a suggestion or motivation for one skilled in the art of multi-threaded execution to look to a reference regarding the recursive splitting of functional units to identify a properly functioning portion to execute instructions during detection of hardware malfunctions. Therefore, Applicants respectfully submit that the Examiner has engaged in an improper hindsight-based analysis to render the above-recited features of Claim 1 obvious over <u>Sager</u> in view of <u>Heath</u>.

Assuming, arguendo, that the Examiner were allowed to rely on the teachings of <u>Sager</u> in view of <u>Heath</u>, Applicants respectfully submit that the recited combination fails to teach each of the above-recited claims features of Claim 1. As indicated above, the teachings of <u>Sager</u> are strictly limited to assigning alternating priority of threads to prevent thread deadlock. Hence, Applicants respectfully submit that the entire specification of <u>Sager</u> is devoid of any teachings with regards to re-execution of instructions. In other words, since <u>Sager</u> provides no teachings or suggestions with regards to re-execution of instructions, one skilled in the art would not modify the thread execution technique as taught by <u>Sager</u> in view of in response to hardware malfunction detection, as taught by Heath.

Accordingly, Applicants respectfully submit that one skilled in the art would not modify the thread execution and alternating thread priority as taught by <u>Sager</u> to re-execute instructions a predetermined number of times, as taught by <u>Heath</u>. Accordingly, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness of Claim 1 over <u>Sager</u> in view of <u>Heath</u> since the combination of references fails to teach each of the above-recited features of Claim 1, and the Examiner fails to illustrate a suggestion or motivation for combining the reference teachings.

Consequently, Applicants respectfully submit that Claim 1 is patentable over the combination of <u>Sager</u> in view of <u>Heath</u>, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 1.

Regarding Clams 2-4 and 6-12, Applicants respectfully submit that Claims 2-4 and 6-12 depend from Claim 1 and therefore include the above-recited claim features of Claim 1. Accordingly, Claims 2-4 and 6-12, based on their dependency from Claim 1, are also patentable over the combination of <u>Sager</u> in view of <u>Heath</u>, as well as the references of record. Consequently,

Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 2-4 and 6-12.

Regarding Claim 19, Claim 19 includes the following claim feature, which is neither taught nor suggested by either <u>Sager</u>, <u>Heath</u> or the references of record:

dispatching one of the plurality of <u>instructions</u> to an execution unit to be executed either <u>when</u> a <u>counter</u> for the instruction does <u>not exceed a maximum number of replays</u> or, if the <u>counter</u> for the instruction <u>exceeds</u> the <u>maximum number of replays</u>, <u>when</u> a <u>required data</u> for the <u>instruction</u> is <u>available</u>. (Emphasis added.)

As indicated above with reference to the Examiner's rejection of Claim 1, the Examiner is prohibited from relying on the combination of <u>Sager</u> in view of <u>Heath</u> since the Examiner has failed to provide to some suggestion or motivation to modify the reference or combine the reference teachings, as required to establish a *prima facie* case of obviousness. Moreover, even assuming the Examiner was allowed to rely on the combination of <u>Sager</u> in view of <u>Heath</u>, the teachings of <u>Heath</u> are strictly limited to:

signaling an operator that corrective action is necessary after a predetermined number of unsuccessful attempts to re-execute the instruction. (*See*, col. 2, lines 10–14.)

Conversely, in such a situation, Claim 19 recites the execution of an instruction when the required data for the instruction is available following a maximum number of replays. Accordingly, even if the Examiner were allowed to rely on the combination of <u>Sager</u> in view of <u>Heath</u>, the combination would teach the notification of an operator once an instruction has been replayed a maximum number of times. Accordingly, the combination would fail to teach each of the above-recited features of Claim 19.

Therefore, Applicants respectfully submit that, for at least the reasons described above, the Examiner fails to establish a *prima facie* case of obviousness of Claim 19 over <u>Sager</u> in view of <u>Heath</u>, since neither <u>Sager</u> nor <u>Heath</u> teach or suggest the aforementioned execution technique for replay of instructions, as recited by Claim 19. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 19.

Regarding Claims 20-24, Claims 20-24 depend from Claim 19 and therefore include the patentable claim features of Claim 19, as described above. Accordingly, Claims 20-24, based on their dependency from Claim 19, and for at least reasons described above, are also patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 20-24.

The Examiner rejects Claims 5 and 21 under 35 U.S.C. §103(a) as being unpatentable over <u>Sager</u> in view of <u>Heath</u>, as applied to Claims 4 and 20, and further in view of U.S. Patent No. 5,944,818 issued to Baxter ("<u>Baxter</u>"). Applicants respectfully traverse this rejection.

Regarding the Examiner's citing of <u>Baxter</u>, Applicants respectfully submit that the Examiner is prohibited from relying on the combination of <u>Sager</u> in view of <u>Heath</u> since the Examiner fails to illustrate some suggestion or motivation for combining the reference teachings. Accordingly, the Examiner would also be prohibited from the combination of <u>Sager</u> in view of <u>Heath</u> and further in view of <u>Baxter</u>.

Even assuming the Examiner were able to rely on the combination, the Examiner's citing of <u>Baxter</u> would fail to rectify deficiencies of the combination of <u>Sager</u> in view of <u>Heath</u> to limit execution of the instruction to when the instruction is safe to execute, as recited by Claim 1, or when a required data for the instruction is available, as recited by Claim 19, once re-execution of the instruction exceeds the maximum number of replays. Accordingly, Applicants respectfully submit that Claims 1 and 19 are both patentable over the combination of <u>Sager</u> in view of <u>Heath</u> and further in view of <u>Baxter</u>, since the combination of references fail to teach or suggest each of the above-recited features of Claims 1 and 19.

Accordingly, Claims 5 and 21, which depend from Claims 1 and 19, respectively, are also patentable over <u>Sager</u> in view of <u>Heath</u> and further in view of <u>Baxter</u>, based on their dependency from Claims 1 and 19, respectively. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Clams 5 and 21.

The Examiner rejects Claims 13-17 under 35 U.S.C. §103(a) as being unpatentable over <u>Sager</u> in view of <u>Heath</u>, and further in view of <u>Superscalar Microprocessor Design</u>, Mike Johnson, Prentice Hall, Inc., 1991 ("<u>Johnson</u>"). Applicants respectfully traverse this rejection.

Regarding Claim 13, Claim 13 includes the following claim feature, which is neither taught nor suggested by the references of record:

at least two schedulers coupled between the replay queue and the execution units to schedule instructions for execution, to <u>increment a counter</u> for each of the plurality of instructions to <u>reflect</u> the <u>number of times</u> each of the plurality of <u>instructions</u> has been <u>executed</u>, and to <u>communicate each instruction</u> of the plurality of instructions to the execution units <u>when the counter does not exceed a maximum number</u> or, if the <u>counter</u> for the instruction <u>exceeds</u> the <u>maximum number</u> of <u>replays</u>, <u>when a data required</u> by the <u>instruction is available</u>. (Emphasis added.)

Regarding the Examiner's citing of <u>Johnson</u>, Applicants respectfully submit that the Examiner is prohibited from relying on the combination of <u>Sager</u> in view of <u>Heath</u> since the Examiner fails to illustrate some suggestion or motivation for combining the reference teachings.

042390.P9576 -12- 09/705,668

Accordingly, the Examiner would also be prohibited from the combination of <u>Sager</u> in view of <u>Heath</u> and further in view of <u>Johnson</u>.

Even assuming the Examiner were able to rely on the combination, the Examiner's citing of <u>Johnson</u> would fail to rectify deficiencies of the combination of <u>Sager</u> in view of <u>Heath</u> to limit execution of the instruction to when the instruction is safe to execute, as recited by Claim 1, or when a required data for the instruction is available, as recited by Claim 13, once re-execution of the instruction exceeds the maximum number of replays. Accordingly, Applicants respectfully submit that Claim 13 is patentable over the combination of <u>Sager</u> in view of <u>Heath</u> and further in view of <u>Johnson</u>, since the combination of references fail to teach or suggest each of the above-recited features of Claim 13.

Consequently, Applicants respectfully submit that for at least the reasons described above, the Examiner fails to establish a *prima facie* case of obviousness of Claim 13 over <u>Sager</u> in view of <u>Heath</u> and further in view of <u>Johnson</u>, since the proposed combination suggested by the Examiner fails to teach the aforementioned scheduler for replay of instructions as required by Claim 13. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 13.

Regarding Claims 14-17, Claims 14-17 depend from Claim 13, and therefore include the patentable claim features of Claim 13, as described above. Accordingly, Claims 14-17, based on their dependency from Claim 13, and for at least the reasons described above, are also patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 14-17.

The Examiner rejects Claim 18 under 35 U.S.C. §103(a) as being unpatentable over <u>Sager</u> in view of <u>Heath</u>, as applied to Claim 17, and further in view of <u>Baxter</u>. Applicants respectfully traverse this rejection.

Regarding the Examiner's citing of <u>Baxter</u>, for at least the reasons indicated above, the Examiner's citing of <u>Baxter</u> fails to rectify the deficiencies of the combination of <u>Sager</u> in view of <u>Heath</u> to teach the above-recited features of Claim 13. Accordingly, Claim 18, based on its dependency from Claim 13, is also similarly patentable over the combination of <u>Sager</u> in view of <u>Heath</u> and further in view of <u>Baxter</u>. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 18.

The Examiner rejects Claims 1-4, 6, 9-12 and 19-24 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,212,626 issued to Merchant et al. ("Merchant") in view of Heath. Applicants respectfully traverse this rejection.

Regarding Claims 1 and 19, Claims 1 and 19 recite techniques for execution of an instruction, which has been replayed a maximum number of times. As recited by Claim 1, an instruction, which has been replayed a maximum number of times, is restricted from execution until the instruction is safe to execute. As recited by Claim 19, the instruction is restricted from executing until required data for the instruction is available.

As indicated above, the teachings of <u>Heath</u> are strictly limited to techniques for executing instructions upon detection of a hardware malfunction by using the recursive splitting of functional units to identify a properly functioning portion. As taught by <u>Heath</u>, when an instruction has been re-executed a predetermined number of times, an operator is notified. Accordingly, Applicants respectfully submit that the combination of <u>Merchant</u> in view of <u>Heath</u> fails to teach each of the above-recited features of Claims 1 and 19 since neither Claim 1 nor Claim 19 recite the notification of an operator once an instruction has been replayed a maximum number of times.

Furthermore, Applicants respectfully submit that the teachings of <u>Merchant</u> are directed to out-of-order processors, as well as re-execution of instructions, which is not due to hardware malfunctions, but instead may be due to invalid data associated with an instruction due to a cache miss. Accordingly, Applicants respectfully submit that one skilled in the art would not look to the teachings of <u>Heath</u> when dealing with out-of-order processors and speculative execution of instructions, since the teachings of <u>Heath</u> are completely devoid of out-of-order processors and speculative execution of instructions.

Therefore, Applicants respectfully submit that the Examiner has failed to illustrate some suggestion or motivation to combine or modify the reference teachings of Merchant in view of Heath, as suggested by the Examiner. Consequently, the above-recited features of Claims 1 and 19 could only be arrived at through inappropriate hindsight.

Accordingly, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness of Claims 1 and 19 over <u>Merchant</u> in view of <u>Heath</u>, since the combination of references fails to recite each of the above-recited claim features of Claims 1 and 19 and the Examiner fails to show some suggestion or motivation for combining the reference teachings. Therefore, Claims 1 and 19 are patentable over the combination of <u>Merchant</u> in view of <u>Heath</u>, as well as the references of record.

Furthermore, 35 U.S.C. §103(c) prohibits the Examiner from citing <u>Merchant</u> to render Claims 1 and 19 obvious. Pursuant to 35 U.S.C. §103(c), (1) <u>Merchant</u> only qualifies as a §102(e) reference and (2) the invention of the pending claims and the invention of <u>Merchant</u> were, at the time the pending claims were made, owned by the same person or subject to an obligation of assignment to the same person. Here, the same person is Intel Corporation of Santa Clara, California. Thus, <u>Merchant</u> cannot properly be cited as a §103(a) reference. Consequently,

042390.P9576 -14- 09/705,668

Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 1 and 19.

The Examiner rejects Claim 5 under 35 U.S.C. §103(a) as being unpatentable over Merchant in view of Heath, as applied to Claims 4 and 20, and further in view of Baxter. Applicants respectfully traverse this rejection.

Regarding the Examiner's citing of <u>Baxter</u>, Applicants respectfully submit that the Examiner is prohibited from relying on the combination of <u>Sager</u> in view of <u>Heath</u> since the Examiner fails to illustrate some suggestion or motivation for combining the reference teachings. Accordingly, the Examiner would also be prohibited from the combination of <u>Sager</u> in view of Heath and further in view of <u>Baxter</u>.

Even assuming the Examiner were able to rely on the combination, the Examiner's citing of <u>Baxter</u> would fail to rectify deficiencies of the combination of <u>Merchant</u> in view of <u>Heath</u> to limit execution of the instruction to when the instruction is safe to execute, as recited by Claim 1, once reexecution of the instruction exceeds the maximum number of replays.

Accordingly, Applicants respectfully submit that Claim 1 is patentable over the combination of Merchant in view of Heath and further in view of Baxter, since the combination of references fail to teach or suggest each of the above-recited features of Claim 5. Therefore, Claim 5 is also patentable over the combination of Merchant in view of Heath and further in view of Baxter, since Claim 5 depends from Claim 1. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 5.

The Examiner rejects Claims 13-17 under 35 U.S.C. §103(a) as being unpatentable over Merchant in view of Heath, and further in view of Johnson. Applicants respectfully traverse this rejection.

Regarding Claim 13, Claim 13 includes the following claim feature, which is neither taught nor suggested by the references of record:

at least two schedulers coupled between the replay queue and the execution units to schedule instructions for execution, to increment a counter for each of the plurality of instructions to reflect the number of times each of the plurality of instructions has been executed, and to communicate each instruction of the plurality of instructions to the execution units when the counter does not exceed a maximum number or, if the counter for the instruction exceeds the maximum number of replays, when a data required by the instruction is available. (Emphasis added.)

Regarding the Examiner's citing of <u>Johnson</u>, Applicants respectfully submit that the Examiner is prohibited from relying on the combination of <u>Merchant</u> in view of <u>Heath</u> since the Examiner fails to illustrate some suggestion or motivation for combining the reference teachings.

042390.P9576 -15- 09/705,668

Accordingly, the Examiner would also be prohibited from the combination of <u>Merchant</u> in view of Heath and further in view of <u>Johnson</u>.

Even assuming the Examiner were able to rely on the combination, the Examiner's citing of <u>Johnson</u> would fail to rectify deficiencies of the combination of <u>Merchant</u> in view of <u>Heath</u> to limit execution of the instruction to when a required data for the instruction is available, as recited by Claim 13, once re-execution of the instruction exceeds the maximum number of replays. Accordingly, Applicants respectfully submit that Claim 1 is patentable over the combination of <u>Merchant</u> in view of <u>Heath</u> and further in view of <u>Johnson</u>, since the combination of references fail to teach or suggest each of the above-recited features of Claim 13.

Consequently, Applicants respectfully submit that for at least the reasons described above, the Examiner fails to establish a *prima facie* case of obviousness of Claim 13 over <u>Merchant</u> in view of <u>Heath</u> and further in view of <u>Johnson</u>, since the proposed combination suggested by the Examiner fails to teach the aforementioned scheduler for replay of instructions as required by Claim 13. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 13.

Regarding Claims 14-17, Claims 14-17 depend from Claim 13, and therefore include the patentable claim features of Claim 13, as described above. Accordingly, Claims 14-17, based on their dependency from Claim 13, and for at least the reasons described above, are also patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 14-17.

The Examiner rejects Claim 18 under 35 U.S.C. §103(a) as being unpatentable over Merchant in view of Heath, as applied to Claim 17, and further in view of Baxter. Applicants respectfully traverse this rejection.

Regarding the Examiner's citing of <u>Baxter</u>, for at least the reasons indicated above, the Examiner's citing of <u>Baxter</u> fails to rectify the deficiencies of the combination of <u>Merchant</u> in view of <u>Heath</u> to teach the above-recited features of Claim 13. Accordingly, Claim 18, based on its dependency from Claim 13, is also similarly patentable over the combination of <u>Merchant</u> in view of <u>Heath</u> and further in view of <u>Baxter</u>. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 18.

### **CONCLUSION**

Applicants have amended the claims to recite features that are not taught or suggested by the references. No new matter is introduced by the Applicants' claim amendments, which are supported in Applicants' specification and are necessary for placing the present application in condition for allowance.

In view of the foregoing, it is believed that all claims now pending, namely Claims 1-9 and 11-24. patentably define the present application over the prior art of record, and are therefore in condition for allowance; and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800, ext. 738.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: September 9, 2004

12400 Wilshire Boulevard Seventh Floor Los Angeles, California 90025 (310) 207-3800 Joseph Lutz, Reg. No. 43.765

CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

September 9, 2004

Marilyn Bass

September 9, 2004